PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10083402	02/27/2002	438	006	2812	EL ARINI

**APPLICANTS: Shimada Yutaka; Mori Yasuhiro; Morita Koyo; Yokoshima Kenji;

**CONTINUING DATA VERIFIED:
None ZE

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 2001-259111 08/29/2001
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PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☒ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☒ yes ☐ no		XA-9629
Verified and Acknowledged Examiners's intials	ZE		

TITLE : Manufacturing method of semiconductor integrated circuit device

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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